Good Display	E paper IC Specifications	SPEC NO	
	IL3895	REV NO	

Good Display Specifications

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Good Display

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Appendix: IC Revision history of ILE3895 Specification

Revision	Change Items	Effective Date
1.0	Advance Information Release	30-Sep-15

CONTENTS

TABLES

FIGURES

1 GENERAL DESCRIPTION

IL3895 is a CMOS active matrix bistable display driver with controller. It consists of 150 source outputs, 250 gate outputs, 1 VCOM and 1 VBD for border that can support a maximum display resolution 150x250.

IL3895 embeds booster, regulators and oscillator. Data/Commands are sent from general MCU through the hardware selectable Serial Peripheral Interface.

2 FEATURES

- Design for dot matrix type active matrix EPD display, support mono color for black/white
- Resolution: 150 source outputs; 250 gate outputs; 1 VCOM; 1VBD for border
- Power supply
  - VCI: 2.4 to 3.7V
  - VDDIO: Connect to VCI
  - VDD: 1.8V, regulate from VCI supply
- Gate driving output voltage:
  - 2 levels output (VGH, VGL)
  - Max 42Vp-p
  - VGH: 22V
  - VGL: -20V
- Source / VBD driving output voltage:
  - 3 levels output (VSH, VSS, VSL)
  - VSH: 15V
  - VSL: -15V
- VCOM output voltage:
  - -3V to -0.2V, voltage adjustment in steps of 100mV
- Built in VCOM sensing
- Source and gate scan direction control
- Low current consumption in deep sleep mode
- On-chip display RAM
- Programmable output waveform allowing flexibility for different applications / environments
- On-chip OTP for storing waveform settings
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- Serial peripheral and I2C interface available
- Available in COG package

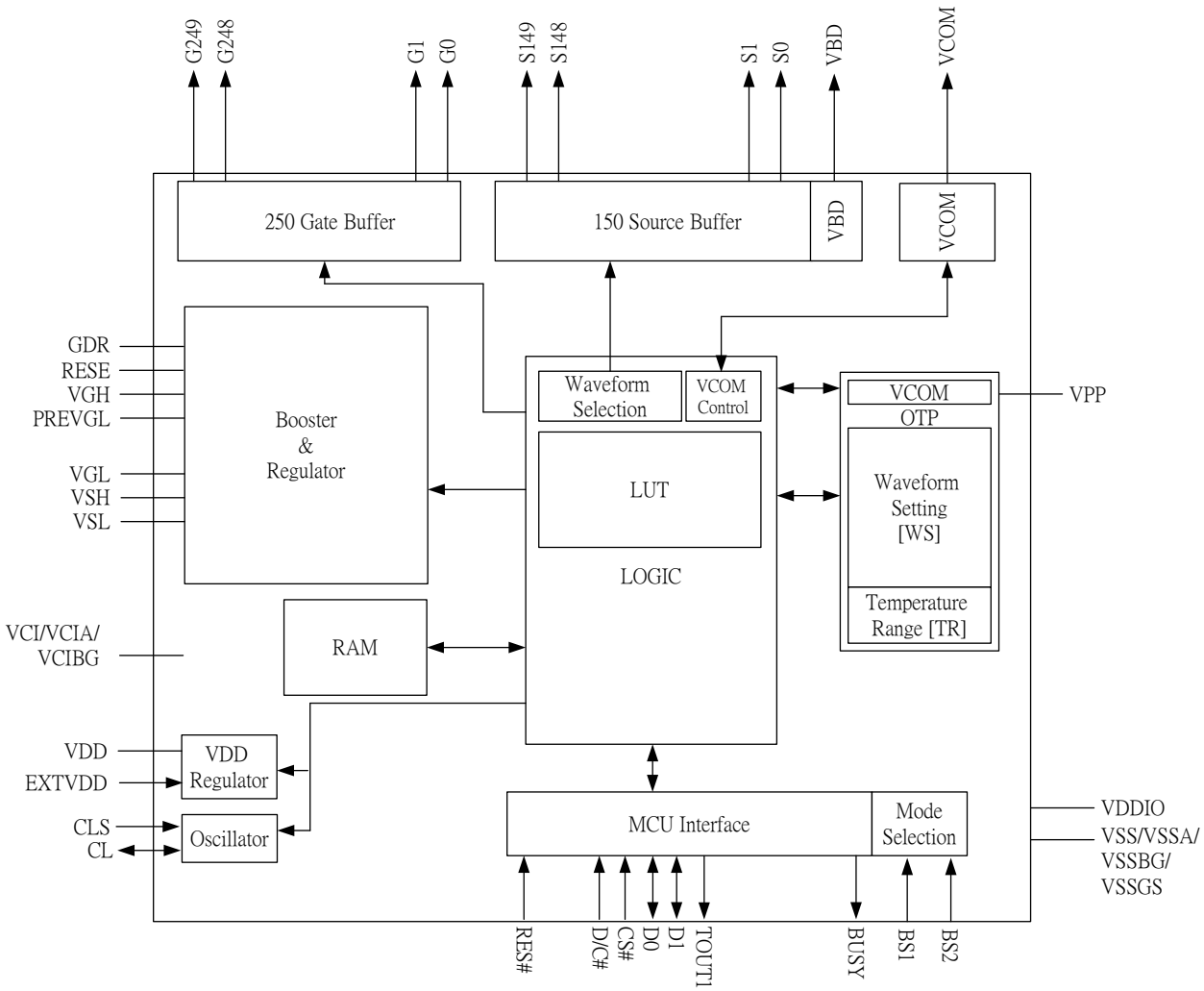
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	Package Form	Remark
IL3895	Gold Bump Die	Bump Face Up On Waffle pack Die thickness: 300um Bump height: 12um

4 BLOCK DIAGRAM

Figure 4-1 : IL3895 Block Diagram



5 PIN DESCRIPTION

Key: I = Input, O =Output, IO = Bi-directional (input/output), P = Power pin, C = Capacitor Pin
NC = Not Connected, Pull L =connect to V_{SS}, Pull H = connect to V_{DDIO}

Pin name	Type	Connect to	Function	Description	When not in use
Input power					
VCI	P	Power Supply	Power Supply	Power input pin for the chip.	-
VCIA	P	Power Supply	Power Supply	Power input pin for the chip. - Connect to VCI in the application circuit.	-
VCIBG	P	Power Supply	Power Supply	Power input for the chip (Reference). - Connect to VCI in the application circuit.	-
VDDIO	P	Power Supply	Power for interface logic pins	Power input pin for the Interface. - Connect to VCI in the application circuit.	-
VDD	P	Capacitor	Regulator output	Core logic power pin. VDD can be regulated internally from VCI. - Connect a stabilizing capacitor between VDD and VSS in the application circuit.	-
EXTVDD	I	VDDIO	Regulator bypass	This pin is VDD regulator bypass pin. - Connect to VSS in the application circuit.	-
VSS	P	VSS	GND	Ground (Digital) pin.	-
VSSA	P	VSS	GND	Ground (Analog) pin. - Connect to VSS in the application circuit.	-
VSSBG	P	VSS	GND	Ground (Reference) pin. - Connect to VSS in the application circuit.	-
VSSGS	P	VSS	GND	Ground (Output) pin. - Connect to VSS in the application circuit.	-
VPP	P	Power Supply	OTP power	Power input pin for OTP Programming.	Open

<table>
<tr><th>Pin name</th><th>Type</th><th>Connect to</th><th>Function</th><th>Description</th><th>When not in use</th></tr>
<tr><td colspan="6">Digital I/O</td></tr>
<tr><td>D [1:0]</td><td>I/O</td><td>MPU</td><td>Data Bus</td><td>Serial clock and data pins for interface:
<table><tr><td>Serial Interface :
- D0: SCLK
- D1: SDIN</td><td>I2C Interface :
- D0: SCL
- D1: SDA_{IN}</td></tr></table></td><td>-</td></tr>
<tr><td>CS#</td><td>I</td><td>MPU</td><td>Logic Control</td><td>Chip selection pin.</td><td>VSS</td></tr>
<tr><td>D/C#</td><td>I</td><td>MPU</td><td></td><td>Data/Command control pin.</td><td>VSS</td></tr>
<tr><td>RES#</td><td>I</td><td>MPU</td><td>System Reset</td><td>Reset signal input pin.
Active Low.</td><td>-</td></tr>
<tr><td>BUSY</td><td>O</td><td>MPU</td><td>Device Busy Signal</td><td>Busy state output pin.
When Busy is High, the operation of the chip should not be interrupted, and command should not be sent.</td><td>Open</td></tr>
<tr><td>CLS</td><td>I</td><td>VDDIO</td><td>Clock Mode Selection</td><td>Internal clock selection pin.
- Connect to VDDIO in the application circuit.</td><td>-</td></tr>
<tr><td>CL</td><td>O</td><td>NC</td><td>Clock signal</td><td>This is the clock signal pin.
The clock signal can be detected at CL.</td><td>-</td></tr>
<tr><td>BS1</td><td>I</td><td>VDDIO/ VSS</td><td>MCU Interface Mode Selection</td><td>MCU interface selection pin.
Table 5-1 : MCU interface selection<table><tr><td>BS2</td><td>BS1</td><td>MCU Interface</td></tr><tr><td>L</td><td>L</td><td>4-wire serial peripheral interface (SPI)</td></tr><tr><td>L</td><td>H</td><td>3-wire serial peripheral interface (SPI) – 9 bits SPI</td></tr><tr><td>H</td><td>L</td><td>I2C Interface</td></tr></table></td><td>-</td></tr>
<tr><td colspan="6">Analog Pin</td></tr>
<tr><td>GDR</td><td>O</td><td>POWER MOSFET Driver Control</td><td>VGH & PREVGL Generation</td><td>N-Channel MOSFET gate drive control pin.</td><td>-</td></tr>
<tr><td>RESE</td><td>I</td><td>Booster Control Input</td><td></td><td>Current sense input pin for the control Loop.</td><td>-</td></tr>
<tr><td>VGH</td><td>C</td><td>Stabilizing capacitor</td><td></td><td>Positive Gate driving voltage and the power input pin for VSH.
- Connect a stabilizing capacitor between VGH and VSS in the application circuit.</td><td>-</td></tr>
<tr><td>PREVGL</td><td>C</td><td>Stabilizing capacitor</td><td></td><td>Power input pin for VGL and VSL.
- Connect a stabilizing capacitor between PREVGL and VSS in the application circuit.</td><td>-</td></tr>
<tr><td>VGL</td><td>C</td><td>Stabilizing capacitor</td><td>VGL Generation</td><td>Negative Gate driving voltage pin.
- Connect a stabilizing capacitor between VGL and VSS in the application circuit.</td><td>-</td></tr>
<tr><td>VSH</td><td>C</td><td>Stabilizing capacitor</td><td>VSH, VSL Generation</td><td>Positive Source driving voltage pin.
- Connect a stabilizing capacitor between VSH and VSS in the application circuit.</td><td>-</td></tr>
<tr><td>VSL</td><td>C</td><td>Stabilizing capacitor</td><td></td><td>Negative Source driving voltage and the power input pin for VCOM.
- Connect a stabilizing capacitor between VSL and VSS in the application circuit.</td><td>-</td></tr>
<tr><td>VCOM</td><td>C</td><td>Panel/ Stabilizing capacitor</td><td>VCOM</td><td>VCOM driving voltage pin.
- Connect a stabilizing capacitor between VCOM and VSS in the application circuit.</td><td>-</td></tr>
</table>

Pin name	Type	Connect to	Function	Description	When not in use
Panel Driving					
S [149:0]	O	Panel	Source driving signal	Source output pin.	Open
G [249:0]	O	Panel	Gate driving signal	Gate output pin.	Open
VBD	O	Panel	Border driving signal	Border output pin.	Open
Data Output Pin					
TOUT1	O	MPU		Data output pin for interface. Serial Interface : Serial data pin for status bit read I2C Interface : SDA_{OUT} When I2C mode is selected, TOUT1, D1 should be tied together and serve as SDA_{out}, SDA_{in} in application	Open
Others					
NC	NC	NC	Not Connected	NC pins. - Keep open. - Don't connect to other NC pins and test pins including TPA, TPB, TPC, TPD, TPF, TIN1 and TIN2.	Open
TPA, TPB, TPC, TPD, TPF	NC	NC	Reserved for Testing	Reserved pins. - Keep open. - Don't connect to other NC pins and test pins including TPA, TPB, TPC, TPD, TPF, TIN1 and TIN2.	Open
TIN	I	NC	Reserved for Testing	Connect to TPE pin.	Tie TIN and TPE together
TPE	O	NC		Connect to TIN pin.	Tie TIN and TPE together
TIN1	I	VDDIO	Reserved for Testing	Reserved pin. - Connect to VDDIO in the application circuit.	VDDIO

6 FUNCTIONAL BLOCK DESCRIPTION

6.1 MCU Interface

6.1.1 MCU Interface selection

The IL3895 can support 3-wire/4-wire serial peripheral interface. In the IL3895, the MCU interface is pin selectable by BS[2:1] pins shown in Table 6-1. .

Table 6-1 : Interface pins assignment under different MCU interface

	Pin Name						
MCU Interface	**BS2**	**BS1**	**RES#**	**CS#**	**D/C#**	**D0**	**D1**
4-wire serial peripheral interface (SPI)	Connect to VSS	Connect to VSS	Required	Required	Required	SCLK	SDIN
3-wire serial peripheral interface (SPI) – 9 bits SPI	Connect to VSS	Connect to VDDIO	Required	Required	Connect to VSS	SCLK	SDIN
I2C Interface	Connect to VDDIO	Connect to VSS	Required	Connect to VSS	Connect to VSS	SCL	SDA_{IN}

6.1.2 MCU Serial Peripheral Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C# and CS#. In SPI mode, D0 acts as SCLK and D1 acts as SDIN. The control pins status in 4-wire SPI in writing command/data is shown in Table 6-2 and the write procedure 4-wire SPI is shown in Figure 6-1.

Table 6-2 : Control pins status of 4-wire SPI

Function	SCLK pin	SDIN pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

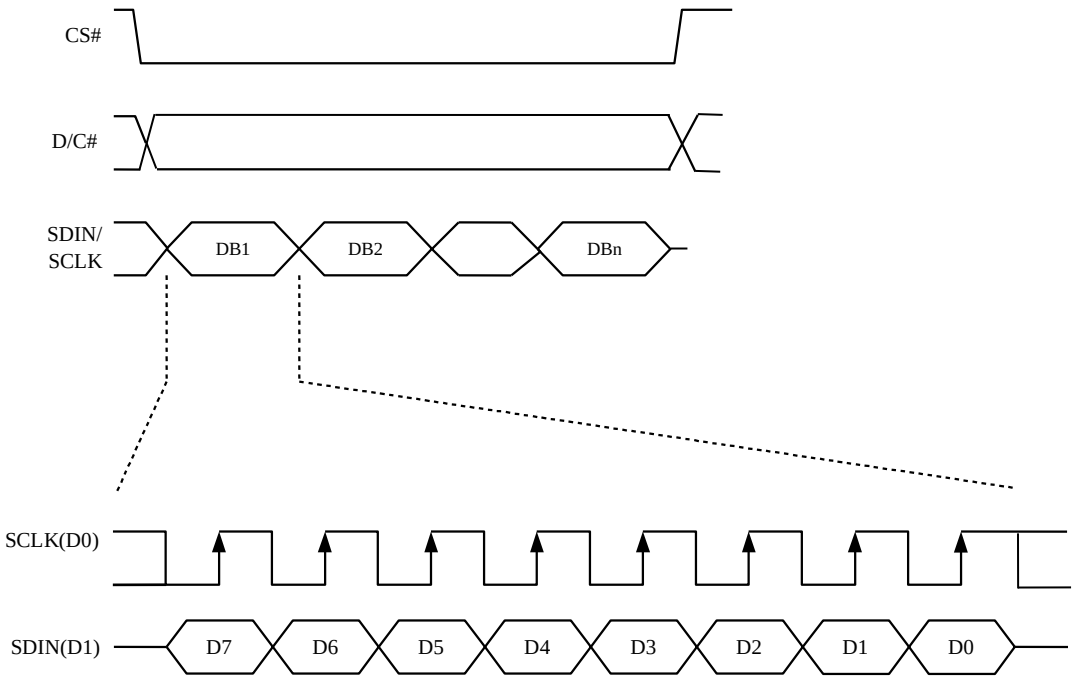
Note:

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

(3) SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

Figure 6-1 : Write procedure in 4-wire SPI



6.1.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCLK, serial data SDIN and CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table 6-3.

In the write operation, a 9-bit data will be shifted into the shift register on every clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Figure 6-2 shows the write procedure in 3-wire SPI

Table 6-3 : Control pins status of 3-wire SPI

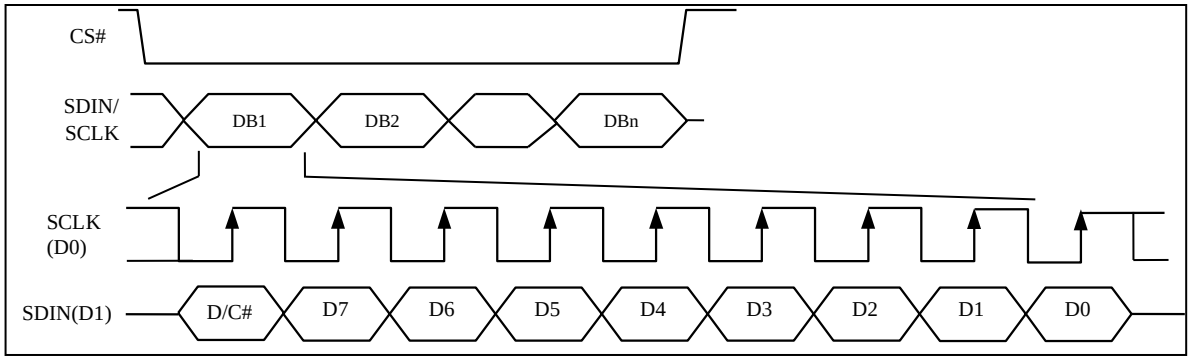
Function	SCLK pin	SDIN pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to V_{SS} and H is connected to V_{DDIO}

(2) ↑ stands for rising edge of signal

Figure 6-2 : Write procedure in 3-wire SPI



6.1.4 MCU I2C Interface

The I^2C communication interface consists of slave address bit SA0, I^2C-bus data signal SDA (SDA_{OUT}/TOUT1 for output) & (SDA_{IN}/D_1 for input) and I^2C-bus clock signal SCL (D_0). Both the data and clock signals must be connected to pull-up resistors. RES# is used for the initialization of device.

a) Slave address bit (SA0)
IL3895 has to recognize the slave address before transmitting or receiving any information by the I^2C-bus. The device will respond to the slave address following by the slave address bit ("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,
b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0
0 1 1 1 1 0 SA0 R/W#
"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of IL3895. D/C# pin acts as SA0 for slave address selection.
"R/W#" bit is used to determine the operation mode of the I^2C-bus interface. R/W#=1, it is in read mode. R/W#=0, it is in write mode.

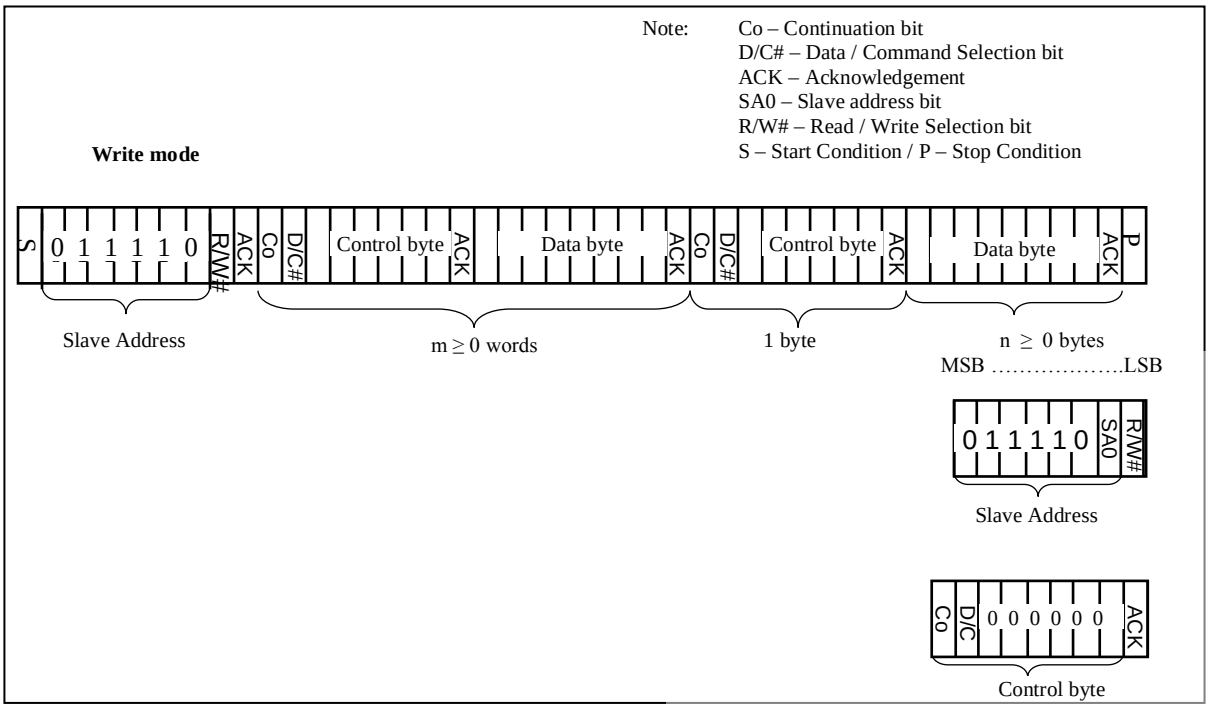
b) I^2C-bus data signal (SDA)
SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.
It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA".
"D1" and "TOUT1" are tied together and serve as SDA. The "D1" pin must be connected to act as SDA. The "TOUT1" pin may be disconnected. When "TOUT1" pin is disconnected, the acknowledgement signal will be ignored in the I^2C-bus.

c) I^2C-bus clock signal (SCL)
The transmission of information in the I^2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.
"D0" serves as SCL.

6.1.4.1 I2C-bus Write data

The I^2C-bus interface gives access to write data and command into the device. Please refer to Figure 6-3 for the write mode of I^2C-bus in chronological order.

Figure 6-3 : I^2C-bus data format



6.1.4.2 Write mode for I2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in Figure 6-4. The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.
2) The slave address is following the start condition for recognition use. For the IL3895, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (D/C pin acts as SA0).
3) The write mode is established by setting the R/W# bit to logic “0”.
4) An acknowledgement signal will be generated after receiving one byte of data, including the slave address and the R/W# bit. Please refer to the Figure 6-5 for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.
5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and D/C# bits following by six “0” ‘s.
    a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.
    b. The D/C# bit determines the next data byte is acted as a command or a data. If the D/C# bit is set to logic “0”, it defines the following data byte as a command. If the D/C# bit is set to logic “1”, it defines the following data byte as a data.
6) Acknowledge bit will be generated after receiving each control byte or data byte.
7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure 6-4. The stop condition is established by pulling the “SDA in” from LOW to HIGH while the “SCL” stays HIGH.

Figure 6-4 : Definition of the Start and Stop Condition

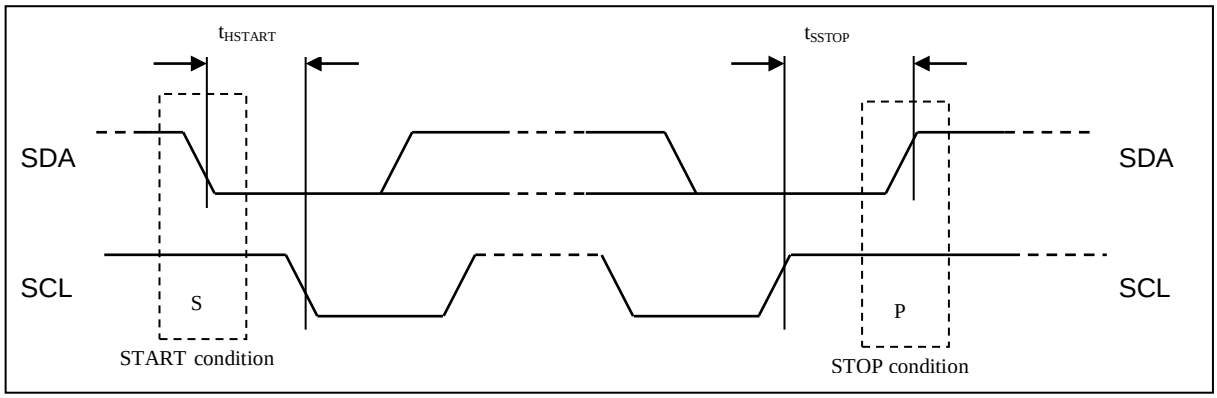
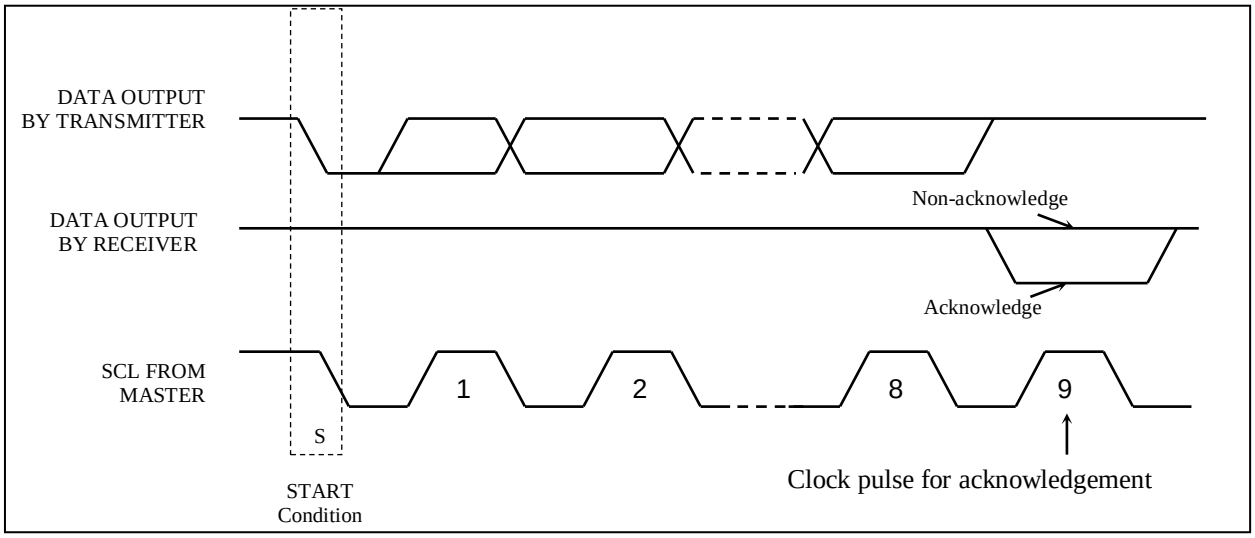


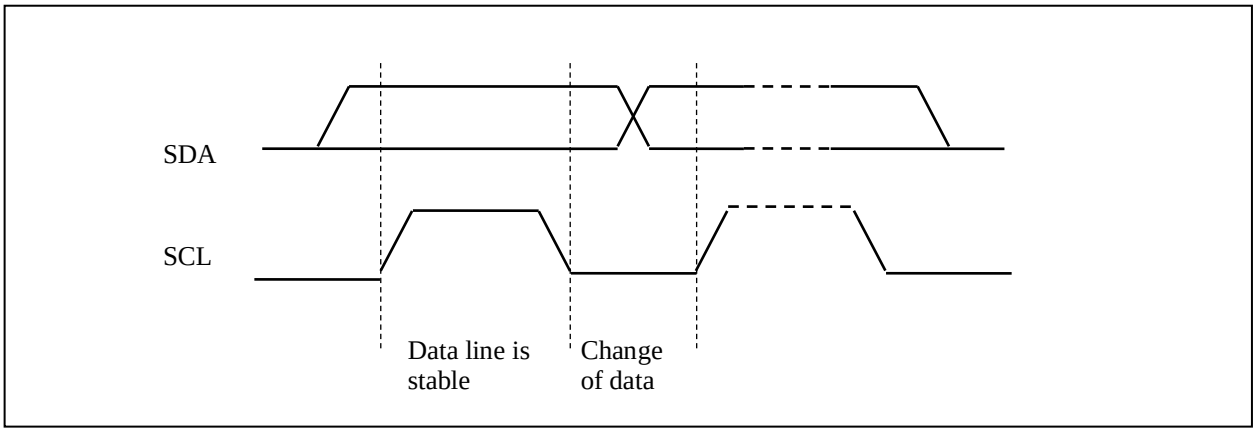
Figure 6-5 : Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the “HIGH” period of the clock pulse. Please refer to the Figure 6-6 for graphical representations. Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure 6-6 : Definition of the data transfer condition



6.2 RAM address map

The on-chip display RAM is used to store the image data for display. There are two sets of display RAM in the IL3895. One set RAM [1] is built for historical data and another set RAM [2] is for the current image data. The size of each RAM set is 150x250 bits.

In order to write the image data into the display RAM, it is necessary to define the Data Entry Mode Setting (Command 0x11h), the Driver Output Control (Command 0x01h) and the Gate Scan Start Position (Command 0x0Fh). The following is an example to show how to set these commands. And, Table 6-4 is the corresponding RAM address mapping of these command settings.

- Command “Data Entry Mode Setting” R11h is set to:

Address Counter update in X direction	AM=0
X: Increment Y: Increment	ID[1:0] =11

- Command “Driver Output Control” R01h is set to:

250 Mux	MUX = F9h
Select G0 as 1st gate	GD = 0
Left and Right gate Interlaced	SM = 0
Scan From G0 to G249	TB = 0

- Command “Gate Scan Start Position” R0Fh is set to:

Set the Start Position of Gate = G0	SCN=0

- Then the data byte sequence: DB0, DB1, DB2 … DB18 … DB19, DB20 … DB4749

Table 6-4 : RAM address map according to above condition

		S0	S1	S2	S3	S4	S5	S6	S7	…	…	S144	S145	S146	S147	S148	S149	XX	XX
		00h								…		12h							
G0	00h	DB0 [7]	DB0 [6]	DB0 [5]	DB0 [4]	DB0 [3]	DB0 [2]	DB0 [1]	DB0 [0]	…	…	DB18 [7]	DB18 [6]	DB18 [5]	DB18 [4]	DB18 [3]	DB18 [2]	DB18 [1]	DB18 [0]
G1	01h	DB19 [7]	DB19 [6]	DB19 [5]	DB19 [4]	DB19 [3]	DB19 [2]	DB19 [1]	DB19 [0]	…	…	DB37 [7]	DB37 [6]	DB37 [5]	DB37 [4]	DB37 [3]	DB37 [2]	DB37 [1]	DB37 [0]
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
G248	F8h	DB4712 [7]	DB4712 [6]	DB4712 [5]	DB4712 [4]	DB4712 [3]	DB4712 [2]	DB4712 [1]	DB4712 [0]	…	…	DB4730 [7]	DB4730 [6]	DB4730 [5]	DB4730 [4]	DB4730 [3]	DB4730 [2]	DB4730 [1]	DB4730 [0]
G249	F9h	DB4731 [7]	DB4731 [6]	DB4731 [5]	DB4731 [4]	DB4731 [3]	DB4731 [2]	DB4731 [1]	DB4731 [0]	…	…	DB4749 [7]	DB4749 [6]	DB4749 [5]	DB4749 [4]	DB4749 [3]	DB4749 [2]	DB4749 [1]	DB4749 [0]
GATE	Y-ADDR																		

Source X-ADDR

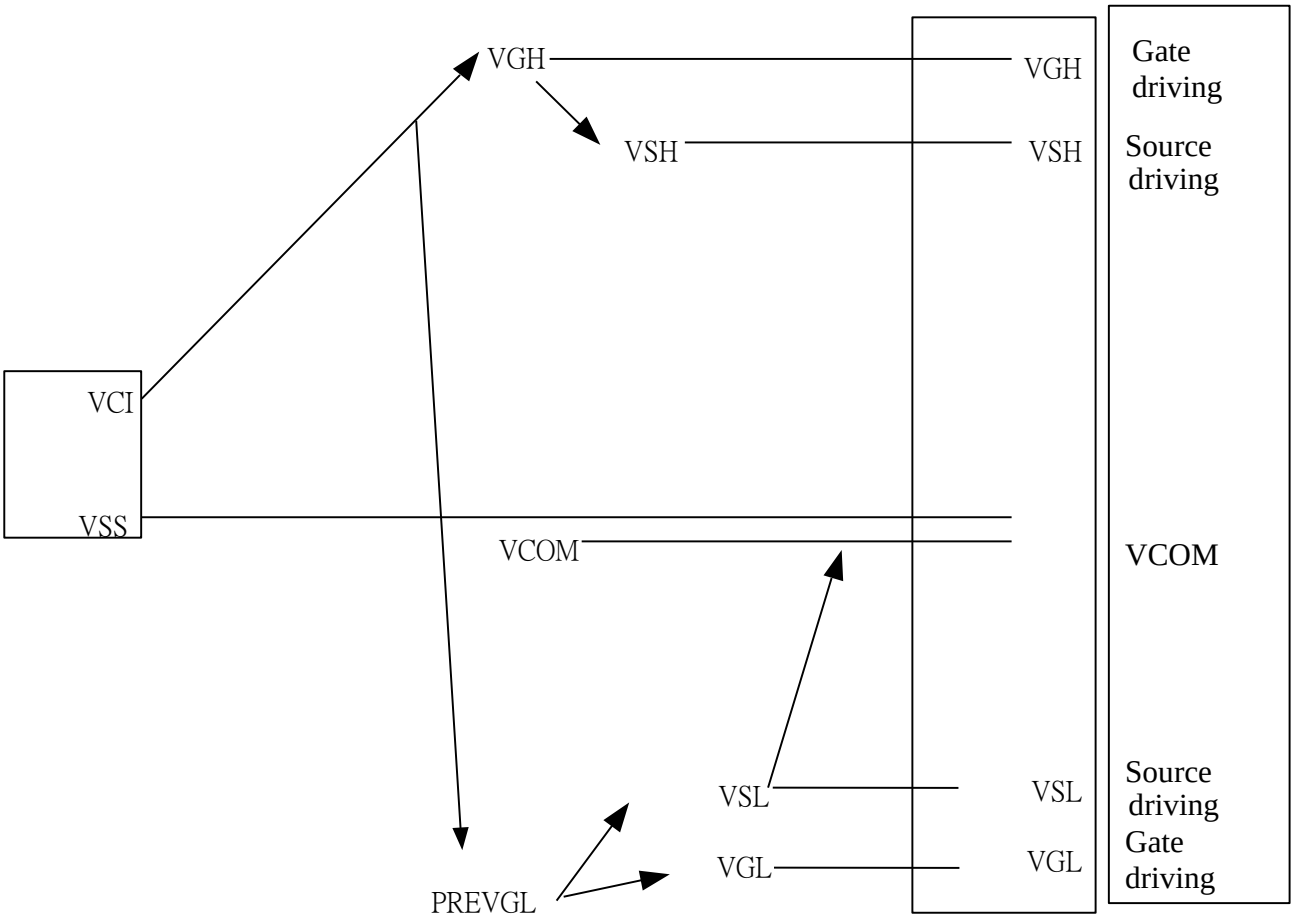
6.3 Oscillator

The on-chip oscillator is included for the use on waveform timing and booster operations. In order to enable the internal oscillator, the CLS pin must be connected to VDDIO.

6.4 Booster & Regulator

A voltage generation system is included in the IL3895 It provides all necessary driving voltages required for an AMEPD panel including VGH, VGL, VSH, VSL and VCOM. Figure 6-3 shows the relation of the voltages. External application circuit is needed to make the on-chip booster & regulator circuit work properly.

Figure 6-7 : Input and output voltage relation chart



- Max voltage difference between VGH and VGL is 42V.

6.5 Panel Driving Waveform

The Vpixel is defined as Figure 6-8, and its relations with GATE, SOURCE are shown Figure 6-5.

Figure 6-8 : Vpixel Definition

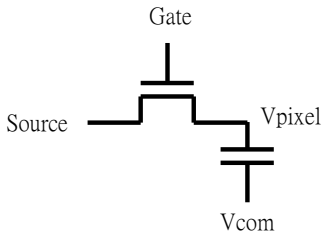
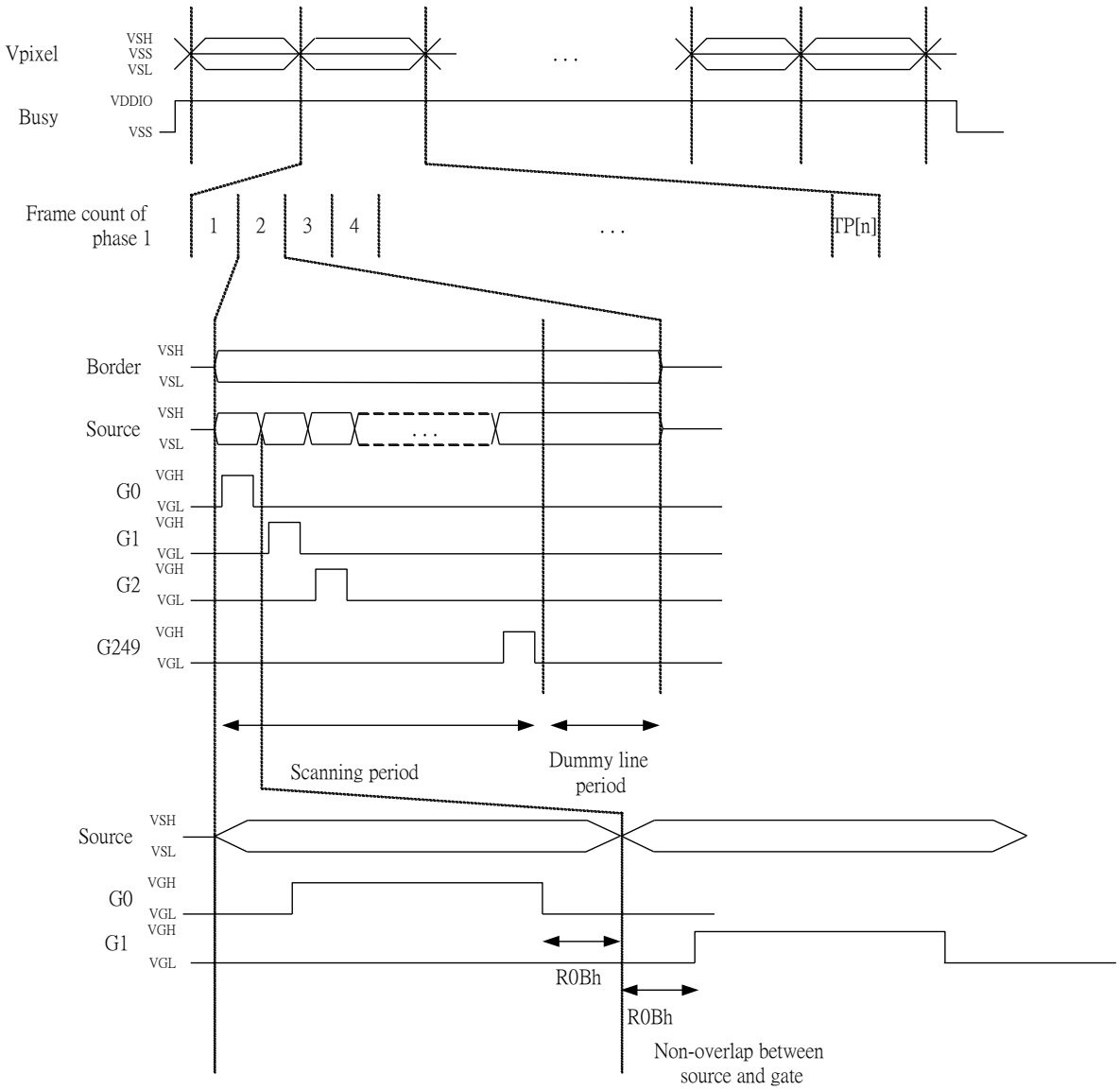


Figure 6-9 : The Relation of Vpixel Waveform with Gate and Source



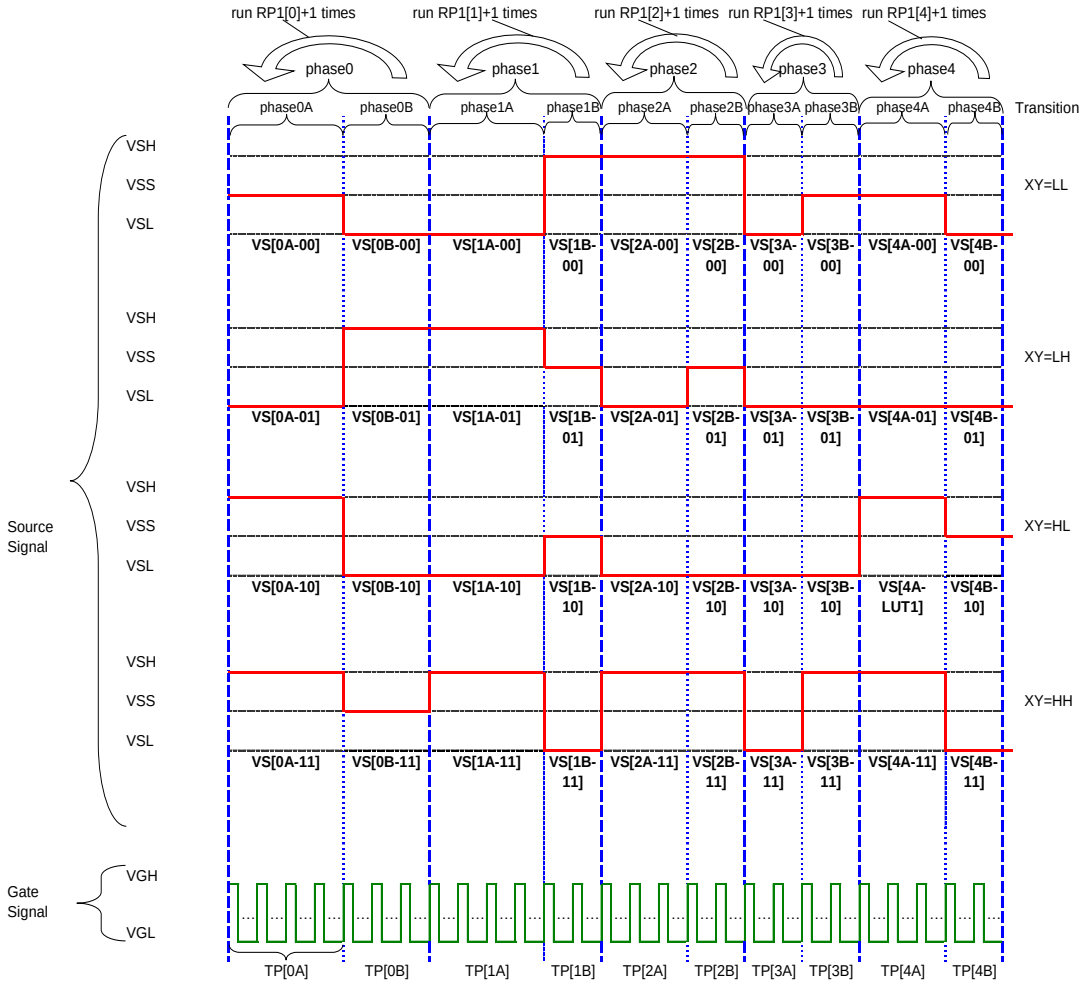
6.6 VCOM Sensing

This functional block provides the scheme to select the optimal VCOM DC level. The VCOM value can be store in the OTP.

6.7 Gate and Programmable Source waveform

Programmable Source waveform of different phase length would be made according to the format of Figure 6-10.

Figure 6-10 : Programmable Source and Gate waveform illustration



- There are totally 10 phases for programmable Source waveform of different phase length.
- The phase period defined as TP [n#] * T_{FRAME}, where TP [n#] range from 0 to 31.
- TP [n#] = 0 indicates phase skipped.
- Source Voltage Level: VS [n#-XY] is constant in each phase.
- The repeat counter defined as RP[n], which represents repeating TP[nA] and TP[nB].
  - RP[n] = 0 indicates run time =1, where RP[n] range from 0 to 63.
- VS [n-XY] indicates the voltage in phase n for transition from X to Y:
  - 00 – VSS
  - 01 – VSH
  - 10 – VSL
- VS [n#-XY] and TP[n#] are stored in waveform lookup table register [LUT].

6.8 Waveform Look Up Table (LUT)

LUT contains 256 bits, which defines the display driving waveform settings. They are arranged in format shown in Figure 6-11.

Figure 6-11 : VS[n-XY] and TP[n] mapping in LUT

in Decimal	D7	D6	D5	D4	D3	D2	D1	D0
0	VS[0A - HH]		VS[0A-HL]		VS[0A - LH]		VS[0A - LL]	
1	VS[0B - HH]		VS[0B - HL]		VS[0B - LH]		VS[0B - LL]	
2	VS[1A - HH]		VS[1A - HL]		VS[1A - LH]		VS[1A - LL]	
3	VS[1B - HH]		VS[1B - HL]		VS[1B - LH]		VS[1B - LL]	
4	VS[2A - HH]		VS[2A - HL]		VS[2A - LH]		VS[2A - LL]	
5	VS[2B - HH]		VS[2B - HL]		VS[2B - LH]		VS[2B - LL]	
6	VS[3A - HH]		VS[3A - HL]		VS[3A - LH]		VS[3A - LL]	
7	VS[3B - HH]		VS[3B - HL]		VS[3B - LH]		VS[3B - LL]	
8	VS[4A - HH]		VS[4A - HL]		VS[4A - LH]		VS[4A - LL]	
9	VS[4B - HH]		VS[4B - HL]		VS[4B - LH]		VS[4B - LL]	
10	0x00							
11	0x00							
12	0x00							
13	0x00							
14	0x00							
15	0x00							
16	RP[0]_ [2:0] Low bits			TP[0A]				
17	RP[0]_ [5:3] High bits			TP[0B]				
18	RP[1]_ [2:0] Low bits			TP[1A]				
19	RP[1]_ [5:3] High bits			TP[1B]				
20	RP[2]_ [2:0] Low bits			TP[2A]				
21	RP[2]_ [5:3] High bits			TP[2B]				
22	RP[3]_ [2:0] Low bits			TP[3A]				
23	RP[3]_ [5:3] High bits			TP[3B]				
24	RP[4]_ [2:0] Low bits			TP[4A]				
25	RP[4]_ [5:3] High bits			TP[4B]				
26	0x00							
27	0x00							
28	0x00							
29		R3A_A[6:0]						
30			R04_A[4:0] - VSH Setting					
31	DUMMY				R3B_A[3:0]			

LUT can be accessed by MCU interface or loaded from OTP.
4 registers are involved to set LUT from MCU interface

- LUT byte 0~28, the content of VS [n-XY], TP [n#], RP[n], are the parameter belonging to Register 0x32:
  - The parameter in bytes 10~15, 26~28 required to be 0x00 for normal operation.
- LUT byte 29, the content of dummy line, is the parameter belonging to Register 0x3A.
- LUT byte 30, the content of source level, is the parameter belonging to Register 0x04.
- LUT byte 31, the content of gate line width, is the parameter belonging to Register 0x3B.

6.9 OTP

6.9.1 The OTP information

The OTP is the non-volatile memory which can store:

- OTP Selection Option
- VCOM value
- Source value
- 7 set of WAVEFORM SETTING (WS) [256bits x 7]
- 6set of TEMPERATURE RANGE (TR) [24bits x 6]

6.9.2 The configuration required for OTP programming

Before programming the OTP with waveform setting ant temperature range, it is necessary to write the WS and the TR data into the on-chip RAM first. The configuration shown in below table must be followed.

Command: Data Entry mode setting	C11, D03	Set Address automatic increment setting = X increment and Y increment Set Address counter update in X direction
Command: RAM X address start /end position	C44, D00, D12	Set RAM Address for S0 to S149
Command: RAM Y address start /end position	C45, D00, DF9	Set RAM Address for G0 to G249
Command: RAM X address counter	C4E, D00	Set RAM X AC as 0
Command: RAM Y address counter	C4F, D00	Set RAM Y AC as 0

For the detail operation flow for OTP programming, please refer to section 9.3 WS OTP Program.

6.9.3 The OTP content and address mapping

The mapping table of OTP is shown in Figure 6-12,

Figure 6-12 : The OTP Content and Address Mapping

Default OTP ADDRESS	SPARE OTP ADDRESS	WRITE RAM ADDRESS X	WRITE RAM ADDRESS Y	D7	D6	D5	D4	D3	D2	D1	D0	
0	256	0	0	VS[0A-HH]		VS[0A-HL]		VS[0A-LH]		VS[0A-LL]		WS [0]
1	257	1	0	VS[0B-HH]		VS[0B-HL]		VS[0B-LH]		VS[0B-LL]		
2	258	0	0	VS[1A-HH]		VS[1A-HL]		VS[1A-LH]		VS[1A-LL]		
3	259	3	0	VS[1B-HH]		VS[1B-HL]		VS[1B-LH]		VS[1B-LL]		
4	260	4	0	VS[2A-HH]		VS[2A-HL]		VS[2A-LH]		VS[2A-LL]		
5	261	5	0	VS[2B-HH]		VS[2B-HL]		VS[2B-LH]		VS[2B-LL]		
6	262	6	0	VS[3A-HH]		VS[3A-HL]		VS[3A-LH]		VS[3A-LL]		
7	263	7	0	VS[3B-HH]		VS[3B-HL]		VS[3B-LH]		VS[3B-LL]		
8	264	8	0	VS[4A-HH]		VS[4A-HL]		VS[4A-LH]		VS[4A-LL]		
9	265	9	0	VS[4B-HH]		VS[4B-HL]		VS[4B-LH]		VS[4B-LL]		
10	266	10	0	0x00								
11	267	11	0	0x00								
12	268	12	0	0x00								
13	269	13	0	0x00								
14	270	14	0	0x00								
15	271	15	0	0x00								
16	272	16	0	RP[0][2:0] Low bits				TP[0A]				
17	273	17	0	RP[0][5:3] High bits				TP[0B]				
18	274	18	0	RP_TP[1]								
19	275	0	1									
20	276	1	1	RP_TP[2]								
21	277	2	1									
22	278	3	1	RP_TP[3]								
23	279	4	1									
24	280	5	1	RP_TP[4]								
25	281	6	1									
26	282	7	1	0x00								
27	283	8	1	0x00								
28	284	9	1	0x00								
29	285	10	1			R3A_A[6:0]						
30	286	11	1			R04_A[4:0] - VSH Setting						
31	287	12	1	DUMMY				R3B_A[3:0]				
32	288	13	1	WS[1]								
63	319	6	3									
				…								
192	448	2	10	WS[6]								
223	479	14	11									
224	480	15	11	TEMP[1L][7:0]								TR1
225	481	16	11	TEMP[1-H][3:0]				TEMP[1L][11:8]				
226	482	17	11	TEMP[1-H][11:4]								
227	483	18	11	TEMP[2L][7:0]								TR2
228	484	0	12	TEMP[2-H][3:0]				TEMP[2L][11:8]				
229	485	1	12	TEMP[2-H][11:4]								
				…								
236	492	8	12	TEMP[5L][7:0]								TR5
237	493	9	12	TEMP[5-H][3:0]				TEMP[5L][11:8]				
238	494	10	12	TEMP[5-H][11:4]								
239	495	11	12	TEMP[6L][7:0]								TR6
240	496	12	12	TEMP[6-H][3:0]				TEMP[6L][11:8]				
241	497	13	12	TEMP[6-H][11:4]								
242	498	14	12	DUMMY								
243	499	15	12	DUMMY								
244	500	16	12	DUMMY								
245	501	17	12	DUMMY								

Remark:

- WS [m] means the waveform setting of temperature set m, the configuration are same as the definition in LUT. The corresponding low temperature range of WS[m] defined as TEMP [m-L] and high range defined as TEMP [m-H]
- Load WS [m] from OTP for LUT if Temp [m-L] < Temperature Register <= Temp [m-H]

6.10 Temperature Searching Mechanism

The OTP waveform mapping is following the mapping in Figure 6-13.

Figure 6-13 : Waveform Setting and Temperature Range # mapping

WS#	Waveform Setting no. #
TR#	Temperature Range no. #
LUT	232 bit register storing the waveform setting (volatile)
Temperature register	12bit Register storing (volatile)
OTP	A non-volatile storing 7 sets of waveform setting and 6 set of temperature range
WS_sel_address	an address pointer indicating the selected WS#

OTP (non-volatile)	
WS0	
WS1	TR1
WS2	TR2
WS3	TR3
WS4	TR4
WS5	TR5
WS6	TR6

Temperature Searching Mechanism:

- Default selection is **WS0**.
- Compare temperature register from **TR1 to TR6**, in sequence. **The last match will be recorded**.
  - i.e., when the temperature register fall in TR3, WS3 will be selected.
  - i.e., when the temperature register fall in TR6, WS6 will be selected.
  - i.e., but when the temperature register fall in both TR3 and TR5, WS5 will be selected.
- If none of the range TR1 to TR6 is match, WS0 will be selected.

User application:

- The default waveform should be programmed as WS0.
- There is no restriction on the sequence of TR1, TR2…. TR6.

6.11 Temperature Register Mapping

1. If the Temperature value MSByte bit D11 = 0, then
The temperature is positive and value (DegC) = + (Temperature value) / 16
2. If the Temperature value MSByte bit D11 = 1, then
The temperature is negative and value (DegC) = ~ (2's complement of Temperature value) / 16

12-bit binary (2's complement)	Hexadecimal Value	Decimal Value	Value [DegC]
0111 1111 0000	7F0	2032	127
0111 1110 1110	7EE	2030	126.875
0111 1110 0010	7E2	2018	126.125
0111 1101 0000	7D0	2000	125
0001 1001 0000	190	400	25
0000 0000 0010	002	2	0.125
0000 0000 0000	000	0	0
1111 1111 1110	FFE	-2	-0.125
1110 0111 0000	E70	-400	-25
1100 1001 0010	C92	-878	-54.875
1100 1001 0000	C90	-880	-55

7 COMMAND TABLE

Table 7-1: Command Table

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[7:0]: MUX Gate lines setting as (A[7:0] + 1) POR = F9h + 1 MUX B[2:0]: Gate scanning sequence and direction B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, … GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, … B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3…G249 (left and right gate interlaced) SM=1, G0, G2, G4 …G248, G1, G3, …G249 B[0]: TB TB = 0 [POR], scan from G0 to G249 TB = 1, scan from G249 to G0.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	B_2	B_1	B_0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate related driving voltage A[4:0] = 10h [POR], VGH at 22V B[3:0] = 0Ah [POR], VGL at -20V
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	B_3	B_2	B_1	B_0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source output voltage magnitude A[4:0] = 19h [POR], VSH/VSL at +/-15V
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	0F	0	0	0	0	1	1	1	1	Gate scan start position	Set the scanning start position of the gate driver. The valid range is from 0 to 249. When TB=0: SCN [7:0] = A[7:0] A[7:0] = 00h [POR] When TB=1: SCN [7:0] = 249 - A[7:0] A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control: A[0] : Description 0 Normal Mode [POR] 1 Enter Deep Sleep Mode
0	1		0	0	0	0	0	0	0	A_0		
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode Note: RAM are unaffected by this command.
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[7:0] – MSByte 01111111[POR] B[7:0] – LSByte 11110000[POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	0	0	0	0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	Option for Display Update Bypass Option used for Pattern Display, which is used for display the RAM content into the Display OLD RAM Bypass option A [7] A[7] = 1: Enable bypass A[7] = 0: Disable bypass [POR] NEW RAM Bypass option A [6] A[6] = 1: Enable bypass A[6] = 0: Disable bypass [POR] A[5] value will be used as Old RAM for bypass. A[5] = 0 [POR] A[4] value will be used as New RAM for bypass. A[4] = 0 [POR] A[3]: the inverse option for OLD RAM A[3] = 1: Enable inverse A[3] = 0: Disable inverse [POR] A[2]: the inverse option for NEW RAM A[2] = 1: Enable inverse A[2] = 0: Disable inverse [POR] A[1:0] Initial Update Option - Source Control:
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[1:0]	Transition	
00	L	L
01 [POR]	L	H
10	H	L
11	H	H

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	22	0	0	1	0	0	0	1	0	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

	Parameter (in Hex)
Enable Clock Signal, Then Enable Analog - Then Load LUT Then INIITIAL DISPLAY Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	FF [POR]
Enable Clock Signal, Then Enable Analog - Then Load LUT Then PATTERN DISPLAY Then Disable Analog Then Disable OSC	F7
To Enable Clock Signal (CLKEN=1)	80
Enable Clock Signal, Then Enable Analog Then PATTERN DISPLAY Then Disable CP Then Disable OSC	C7
To Enable Clock Signal, then Enable Analog (CLKEN=1, CPEN=1)	C0
To INITIAL DISPLAY + PATTEN DISPLAY	0C
To INITIAL DISPLAY	08
To DISPLAY PATTEN	04
To Disable Analog, then Disable Clock Signal (CLKEN=1, CPEN=1)	03
To Disable Clock Signal (CLKEN=1)	01

Remark:
CLKEN=1:
If CLS=VDDIO then Enable OSC.
CLKEN=0:
If CLS=VDDIO then Disable OSC.

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	24	0	0	1	0	0	1	0	0	Write RAM	After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabling time between entering VCOM sensing mode and reading acquired. VCOM sense duration = Setting + 1 Seconds A[3:0] = 09h [POR], duration = 10s.
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

A[7:0]	VCOM	A[7:0]	VCOM
0Fh	-0.2	5Ah	-1.7
14h	-0.3	5Fh	-1.8
19h	-0.4	64h	-1.9
1Eh	-0.5	69h	-2
23h	-0.6	6Eh	-2.1
28h	-0.7	73h	-2.2
2Dh	-0.8	78h	-2.3
32h	-0.9	7Dh	-2.4
37h	-1	82h	-2.5
3Ch	-1.1	87h	-2.6
41h	-1.2	8Ch	-2.7
46h	-1.3	91h	-2.8
4Bh	-1.4	96h	-2.9
50h	-1.5	9Bh	-3
55h	-1.6		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	A[1:0]: Chip ID (POR=01)
1	1		0	0	0	0	0	0	A_1	A_0		
0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [29 bytes], which contains the content of VS [n-XY], TP [n#], RP[n].
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		:	:	:	:	:	:	:	:		
0	1		.	..	.	.	.	.	.	.		
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h]
0	0	37	0	0	1	1	0	1	1	1	OTP selection Control	Write the OTP Selection: A[7]=1 spare VCOM OTP A[6] VCOM_Status A[5]=1 spare WS OTP A[4] WS_Status A[3:0] are reserved OTP bit. User can treat the bits as Version Control.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set number of dummy line period A[6:0]: Number of dummy line period in term of TGate A[6:0] = 06h [POR] Available setting 0 to 127.
0	1		0	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set Gate line width (TGate) A[3:0] Line width in us A[3:0] | TGate / us 1011 | 78 [POR] Remark: Default value will give 50Hz Frame frequency under 6 dummy line pulse setting.
0	1		0	0	0	0	A_3	A_2	A_1	A_0		
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A [7] Follow Source at Initial Update Display A [7]=0: [POR] A [7]=1: Follow Source at Initial Update Display for VBD, A [6:0] setting are being overridden at Initial Display STAGE. A [6] Select GS Transition/ Fix Level for VBD A [6]=0: Select GS Transition A[3:0] for VBD A [6]=1: Select FIX level Setting A[5:4] for VBD [POR] A [5:4] Fix Level Setting for VBD A[5:4] | VBD level 00 | VSS 01 | VSH 10 | VSL 11[POR] | HiZ A [1:0] transition setting for VBD (Select waveform like data A[3:2] to data A[1:0]) A[1:0] | Transition 00 | L | L 01 [POR] | L | H 10 | H | L 11 | H | H
0	1		A_7	A_6	A_5	A_4	0	0	A_1	A_0		

Command Table												
R/W#	**D/C#**	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0]: X-Start, POR = 00h B[4:0]: X-End, POR = 12h
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[7:0]: Y-Start, POR = 00h B[7:0]: Y-End, POR = F9h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0]: POR is 00h.
0	1		0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[7:0]: POR is 00h.
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

8 COMMAND DESCRIPTION

8.1 Driver Output Control (01h)

This double byte command has multiple configurations and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MUX[7]	MUX[6]	MUX[5]	MUX[4]	MUX[3]	MUX[2]	MUX[1]	MUX[0]
POR		1	1	1	1	1	0	0	1
W	1						GD	SM	TB
POR							0	0	0

MUX[7:0]:
Specify number of lines for the driver: MUX[7:0] + 1. Multiplex ratio (MUX ratio) from 16 MUX to 250MUX.

GD:
Selects the 1st output Gate
This bit is made to match the GATE layout connection on the panel. It defines the first scanning line.

SM:
Change scanning order of gate driver.
When SM is set to 0, left and right interlaced is performed.
When SM is set to 1, no splitting odd / even of the GATE signal is performed,
Output pin assignment sequence is shown as below (for 250 MUX ratio):

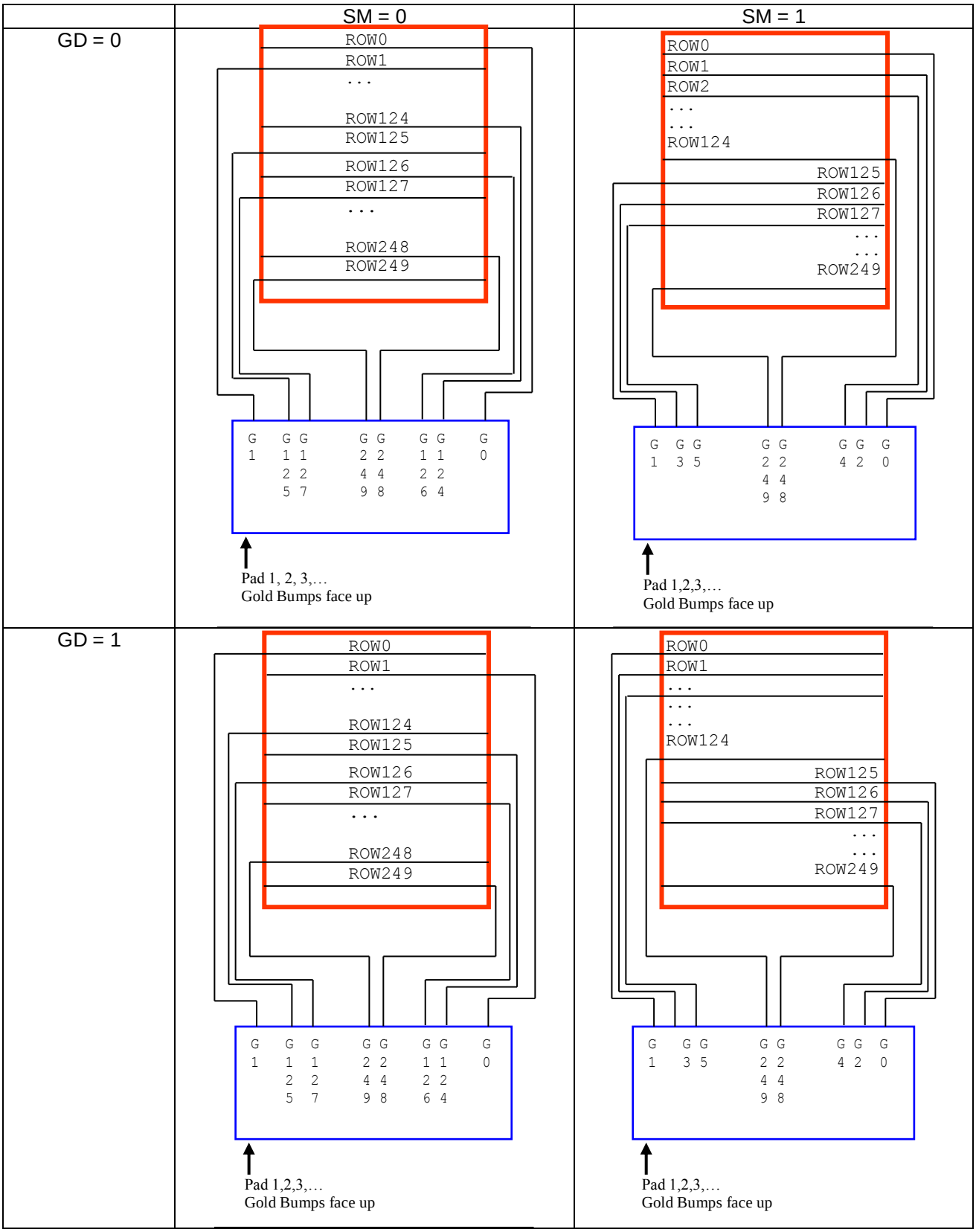
	SM=0	SM=0	SM=1	SM=1
Driver	**GD=0**	**GD=1**	**GD=0**	**GD=1**
G0	ROW0	ROW1	ROW0	ROW125
G1	ROW1	ROW0	ROW125	ROW0
G2	ROW2	ROW3	ROW1	ROW126
G3	ROW3	ROW2	ROW126	ROW1
:	:	:	:	:
G123	ROW123	ROW122	ROW186	ROW61
G124	ROW124	ROW125	ROW62	ROW187
G125	ROW125	ROW124	ROW187	ROW62
G126	ROW126	ROW127	ROW63	ROW188
:	:	:	:	:
G246	ROW246	ROW247	ROW123	ROW248
G247	ROW247	ROW246	ROW248	ROW123
G248	ROW248	ROW249	ROW124	ROW249
G249	ROW249	ROW248	ROW249	ROW124

See “Scan Mode Setting” on next page.

TB:
Change scanning direction of gate driver.
This bit defines the scanning direction of the gate for flexible layout of signals in module either from up to down (TB = 0) or from bottom to up (TB = 1).

The output pin assignment on different scan mode setting is shown in Figure 8-1.

Figure 8-1: Output pin assignment on different Scan Mode Setting



8.2 Gate Scan Start Position (0Fh)

This command is to set Gate Start Position for determining the starting gate of display RAM by selecting a value from 0 to 249 and each bit setting is described as follows:

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
POR		0	0	0	0	0	0	0	0

Figure 8-2 shows an example using this command of this command when MUX ratio= 250 and MUX ratio= 125 “ROW” means the graphic display data RAM row.

Figure 8-2: Example of Set Display Start Line with no Remapping

	MUX ratio (01h) = F9h	MUX ratio (01h) = 7Ch	MUX ratio (01h) = 7Ch
GATE Pin	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 000h	Gate Start Position (0Fh) = 046h
G0	ROW0	ROW0	-
G1	ROW1	ROW1	-
G2	ROW2	ROW2	-
G3	ROW3	ROW3	-
:	:	:	:
:	:	:	:
G68	:	:	-
G69	:	:	-
G70	:	:	ROW70
G71	:	:	ROW71
:	:	:	:
:	:	:	:
G123	ROW123	ROW123	:
G124	ROW124	ROW124	:
G125	ROW125	-	:
G126	ROW126	-	:
:	:	:	:
:	:	:	:
G193	:	:	ROW193
G194	:	:	ROW194
G195	:	:	-
G196	:	:	-
:	:	:	:
:	:	:	:
G246	ROW246	-	-
G247	ROW247	-	-
G248	ROW248	-	-
G249	ROW249	-	-
Display Example			

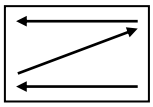
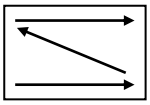
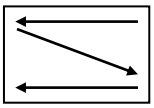
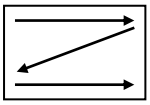
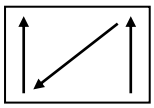
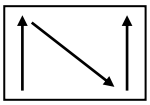
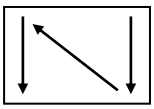
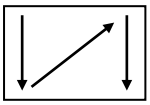
8.3 Data Entry Mode Setting (11h)

This command has multiple configurations and each bit setting is described as follows:

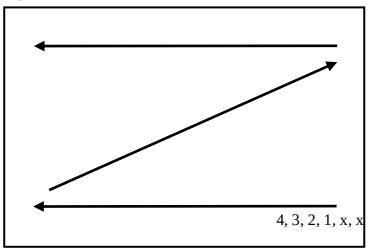
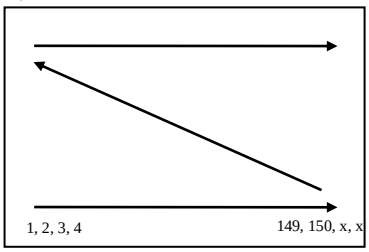
R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1						AM	ID1	ID0
POR		0	0	0	0	0	0	0	0

ID[1:0]: The address counter is automatically incremented by 1, after data is written to the RAM when ID[1:0] = “01”. The address counter is automatically decremented by 1, after data is written to the RAM when ID[1:0] = “00”. The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. The direction of the address when data is written to the RAM is set by AM bits.

AM: Set the direction in which the address counter is updated automatically after data are written to the RAM. When AM = “0”, the address counter is updated in the X direction. When AM = “1”, the address counter is updated in the Y direction. When window addresses are selected, data are written to the RAM area specified by the window addresses in the manner specified with ID[1:0] and AM bits.

	ID [1:0]="00” X: decrement Y: decrement	ID [1:0]=“01” X: increment Y: decrement	ID [1:0]="10” X: decrement Y: increment	ID [1:0]="11” X: increment Y: increment
AM="0” X-mode	00,00h  12, F9h	00,00h  12, F9h	00,00h  12, F9h	00,00h  12, F9h
AM="1” Y-mode	00,00h  12, F9h	00,00h  12, F9h	00,00h  12, F9h	00,00h  12, F9h

The pixel sequence is defined by the ID [0],

	ID[1:0]="00” X: decrement Y: decrement	ID[1:0]="01” X: increment Y: decrement
AM="0” X-mode	00,00h  4, 3, 2, 1, x, x 12, F9h	00,00h  1, 2, 3, 4 149, 150, x, x 12, F9h

8.4 Set RAM X - Address Start / End Position (44h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1				XSA4	XSA3	XSA2	XSA1	XSA0
POR		0	0	0	0	0	0	0	0
W	1				XEA4	XEA3	XEA2	XEA1	XEA0
POR		0	0	0	1	0	0	1	0

XSA[4:0]/XEA[4:0]: Specify the start/end positions of the window address in the X direction by 8 times address unit. Data is written to the RAM within the area determined by the addresses specified by XSA [4:0] and XEA [4:0]. These addresses must be set before the RAM write.
It allows on XEA [4:0] ≤ XSA [4:0]. The settings follow the condition on 00h ≤ XSA [4:0], XEA [4:0] ≤ 12h. The windows is followed by the control setting of Data Entry Setting (R11h)

8.5 Set RAM Y - Address Start / End Position (45h)

R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	YSA7	YSA6	YSA5	YSA4	YSA3	YSA2	YSA1	YSA0
POR	0	0	0	0	0	0	0	0	0
W	1	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0
POR		1	1	1	1	1	0	0	1

YSA[7:0]/YEA[7:0]: Specify the start/end positions of the window address in the Y direction by an address unit. Data is written to the RAM within the area determined by the addresses specified by YSA [7:0] and YEA [7:0]. These addresses must be set before the RAM write.
It allows YEA [7:0] ≤ YSA [7:0]. The settings follow the condition on 00h ≤ YSA [7:0], YEA [7:0] ≤ F9h. The windows is followed by the control setting of Data Entry Setting (R11h)

8.6 Set RAM Address Counter (4Eh-4Fh)

Reg#	R/W	DC	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
4Eh	W	1				XAD4	XAD3	XAD2	XAD1	XAD0
	POR		0	0	0	0	0	0	0	0
4Fh	W	1	YAD7	YAD6	YAD5	YAD4	YAD3	YAD2	YAD1	YAD0
	POR		0	0	0	0	0	0	0	0

XAD[4:0]: Make initial settings for the RAM X address in the address counter (AC).
YAD[7:0]: Make initial settings for the RAM Y address in the address counter (AC).

After RAM data is written, the address counter is automatically updated according to the settings with AM, ID bits and setting for a new RAM address is not required in the address counter. Therefore, data is written consecutively without setting an address. The address counter is not automatically updated when data is read out from the RAM. RAM address setting cannot be made during the standby mode. The address setting should be made within the area designated with window addresses which is controlled by the Data Entry Setting (R11h) {AM, ID[1:0]} ; RAM Address XStart / XEnd Position (R44h) and RAM Address Ystart /Yend Position (R45h). Otherwise undesirable image will be displayed on the Panel.

9 Typical Operating Sequence

9.1 Normal Display

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply);	
2	User	-	HW Reset	
	User	C 12	Command: SW Reset	
	IC		After HW reset, the IC will have Registers load with POR value Ready for command input VCOM register loaded with OTP value IC enter idle mode	BUSY = H
	User	-	Wait until BUSY = L	
3		-	Send initial code to driver including setting of	
	User	C 01	Command: Driver Output Control (MUX, Source gate scanning direction)	
	User	C 3A	Command: Set dummy line period	
	User	C 3B	Command: Set Gate line width	
	User	C 3C	Command: Border waveform control	
4		-	Data operations	
	User	C 11	Command: Data Entry mode setting	
	User	C 44	Command: RAM X address start /end position	
	User	C 45	Command: RAM Y address start /end position	
	User	C 4E	Command: RAM X address counter	
	User	C 4F	Command: RAM Y address counter	
	User	C 24	Command: write RAM	
			Ram Content for Display	
5	User	C 22	Command: Display Update Control 2	BUSY = H
	User	C 20	Command: Master Activation	
	IC	-	Booster and regulators turn on	
	IC	-	Load LUT register with corresponding waveform setting stored in OTP)	
	IC	-	Send output waveform according initial update option	
	IC	-	Send output waveform according to data	
	IC	-	Booster and Regulators turn off	
	IC	-	Back to idle mode	
	User	-	Wait until BUSY = L	
6	User	-	IC power off;	

9.2 VCOM OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI and VPP supply)	
2	User	-	HW Reset	
	User	C 12	Command: SW Reset	BUSY = H
	User	-	Wait until BUSY = L	
3	User	C 22 D 80 C 20	Command: Display Update Control 2 and Master Activation (Enable clock signal)	BUSY = H
	User	-	Wait until BUSY = L	
4	User	C 37	Proceed OTP sequence. Command: OTP selection Control (default or spare)	OTP selection register
5	User	C 36	Command: Program OTP selection	BUSY = H
	User	-	Wait until BUSY = L	
	User	-	Power OFF (VPP supply)	
6		-	Send initial code to driver including setting of (or leave as POR)	VCOM sensing should have same setting during application
	User	C 22 D 40	Command: Display Update Control 2 (Booster on and High voltage ready)	
	User	C 01	Command: Driver Output Control (MUX, Source gate scanning direction)	
	User	C 03	Command: Gate Driving voltage Control	
	User	C 04	Command: Source Driving voltage Control	
	User	C 3A	Command: Set dummy line period	
	User	C 3B	Command: Set Gate line width	
	User	C 32	Command: Write LUT register VCOM sense required full set of LUT for operation, USER required writing LUT in register 32h	
		-	LUT parameter	
	User	C 20	Command: Master Activation Perform the turn off analog operation (assigned by R22h) [Enable Analog blocks]	BUSY = H
	User	-	Wait until BUSY = L	
7	User	C 29	Command: VCOM Sense Duration	
8	User	C 28	Command: VCOM sense	BUSY = H
	IC	-	VCOM pin in sensing mode	
	IC	-	All Source cell have VSS output	
			All Gate scanning continuously	
	IC	-	According to R29h	
	IC	-	Detect VCOM voltage and store in register	
	IC	-	All Gate Stop Scanning.	
	User	-	Wait until BUSY = L	
9	User	C 22 D 02 C 20	Command: Display Update Control 2 and Master Activation (Booster and High voltage disable)	BUSY = H
	User	-	Wait until BUSY = L	
	User	-	Power On (VPP supply)	
10	User	C 2A	Command: Program VCOM OTP	BUSY = H
	User	-	Wait until BUSY = L	
11	User	C 22 D 01 C 20	Command: Display Update Control 2 and Master Activation (Disable clock signal)	BUSY = H
	User	-	Wait until BUSY = L	
12	User	-	IC power off (VCI and VPP Supply)	

9.3 WS OTP Program

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply)	
2	User	-	Power on (VPP supply)	
3	User	-	HW Reset	
	User	C 12	Command: SW Reset	BUSY = H
	User	-	Wait until BUSY = L	
4	User	C 22 D 80 C 20	Command: Display Update Control 2 and Master Activation (Enable clock signal)	BUSY = H
	User	-	Wait BUSY = L	
5	User	C 11 D 03	Command: Data Entry mode setting Set Address automatic increment setting = X increment and Y increment Set Address counter update in X direction	
6	User	C 44 D 00 D 12	Command: RAM X address start /end position Set RAM X address start /end from S0 to S149	
7	User	C 45 D 00 D F9	Command: RAM Y address start /end position Set RAM Y address start /end from G0 to G249	
8	User	C 4E D 00	Command: RAM X address counter Set RAM X address counter as 0	
9	User	C 4F D 00	Command: RAM Y address counter Set RAM Y address counter as 0	
10	User	C 37	Proceed OTP sequence. Command: OTP selection Control (default or spare)	OTP selection register
11	User	C 36	Command: Program OTP selection	BUSY = H
	User	-	Wait BUSY = L	
12	User	C 24	Write corresponding data into RAM	
			Following specific format	
			Write into RAM	
			Full LUT	
13	User	C 4E D 00 C 4F D 00	Command: RAM address start /end position (Initial Ram address counter)	
14	User	C 30	Command: Program WS OTP Waveform Setting OTP programming	BUSY = H
	User	-	Wait BUSY = L	
15	User	C 22 D 01 C 20	Command: Display Update Control 2 and Master Activation (Disable clock signal)	BUSY = H
	User	-	Wait BUSY = L	
16	User	-	Power off VPP and VCI	

10 ABSOLUTE MAXIMUM RATING

Table 10-1: Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CI}	Logic supply voltage	-0.5 to +4.0	V
V_{IN}	Logic Input voltage	-0.5 to V_{DDIO}+0.5	V
V_{OUT}	Logic Output voltage	-0.5 to V_{DDIO}+0.5	V
T_{OPR}	Operation temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} be constrained to the range $V_{SS} < V_{CI}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DDIO}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 11-1: DC Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
V_{SS}	Ground				0		V
V_{CI}	VCI operation voltage		VCI	2.4	3.0	3.7	V
V_{DD}	VDD operation voltage		VDD	1.7	1.8	1.9	V
V_{COM}	VCOM output voltage		VCOM	-3.0		-0.2	V
V_{GATE}	Gate output voltage		G0-249	-20		+22	V
$V_{GATE(p-p)}$	Gate output peak to peak voltage		G0-249			42	V
V_{SH}	Positive Source output voltage		S0-149		+15		V
V_{SL}	Negative Source output voltage		S0-149		-VSH		V
V_{IH}	High level input voltage	VCI = VDDIO		$0.8V_{DDIO}$			V
V_{IL}	Low level input voltage	VCI = VDDIO				$0.2V_{DDIO}$	V
V_{OH}	High level output voltage	VCI = VDDIO IOH = -100uA		$0.9V_{DDIO}$			V
V_{OL}	Low level output voltage	VCI = VDDIO IOL = 100uA				$0.1V_{DDIO}$	V
V_{PP}	OTP Program voltage		VPP	7.25	7.5	7.75	V
DIslp_VCI	Deep sleep mode current	- DC/DC off - No clock, - No output load - No MCU interface access - RAM data retain only and cannot access the RAM	VCI		2	5	uA
Islp_VCI	Sleep mode current	- DC/DC off - No clock - No output load - MCU interface access - RAM data access	VCI		35	50	uA

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Iopr_VCI	Operating current	- DC/DC on - VGH=22V - VGL=-20V - VSH=15V - VSL=-15V - VCOM = -2V - No waveform transitions. - No loading. - No RAM read/write - No OTP read /write - Osc on - Bandgap on	VCI		2000		uA
V_{GH}	Operating Mode Output Voltage	VCI=3.0V DC/DC on VGH=22V VGL=-20V VSH=15V VSL=-15V VCOM = -2V No waveform transitions. No loading. Osc on Bandgap on	VGH	21	22	23	V
V_{SH}			VSH	14.5	15	15.5	V
V_{COM}			VCOM	-2.5	-2	-1.5	V
V_{SL}			VSL	-15.5	-15	-14.5	V
V_{GL}			VGL	-21	-20	-19	V

Table 11-2: Regulators Characteristics

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
IVGH	VGH current	VGH = 22V	VGH			300	uA
IVGL	VGL current	VGL = -20V	VGL			300	uA
IVSH	VSH current	VSH = +15V	VSH			750	uA
IVSL	VSL current	VSL = -15V	VSL			750	uA
IVCOM	VCOM current	VCOM = -2V	VCOM			100	uA

12 AC CHARACTERISTICS

12.1 Oscillator frequency

The following specifications apply for: VSS=0V, VCI=3.0V, VDD=1.8V, T_{OPR}=25ºC.

Table 12-1: Oscillator Frequency

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.4 to 3.7V	CL	0.95	1	1.05	MHz

12.2 Interface Timing

12.2.1 Serial Peripheral Interface

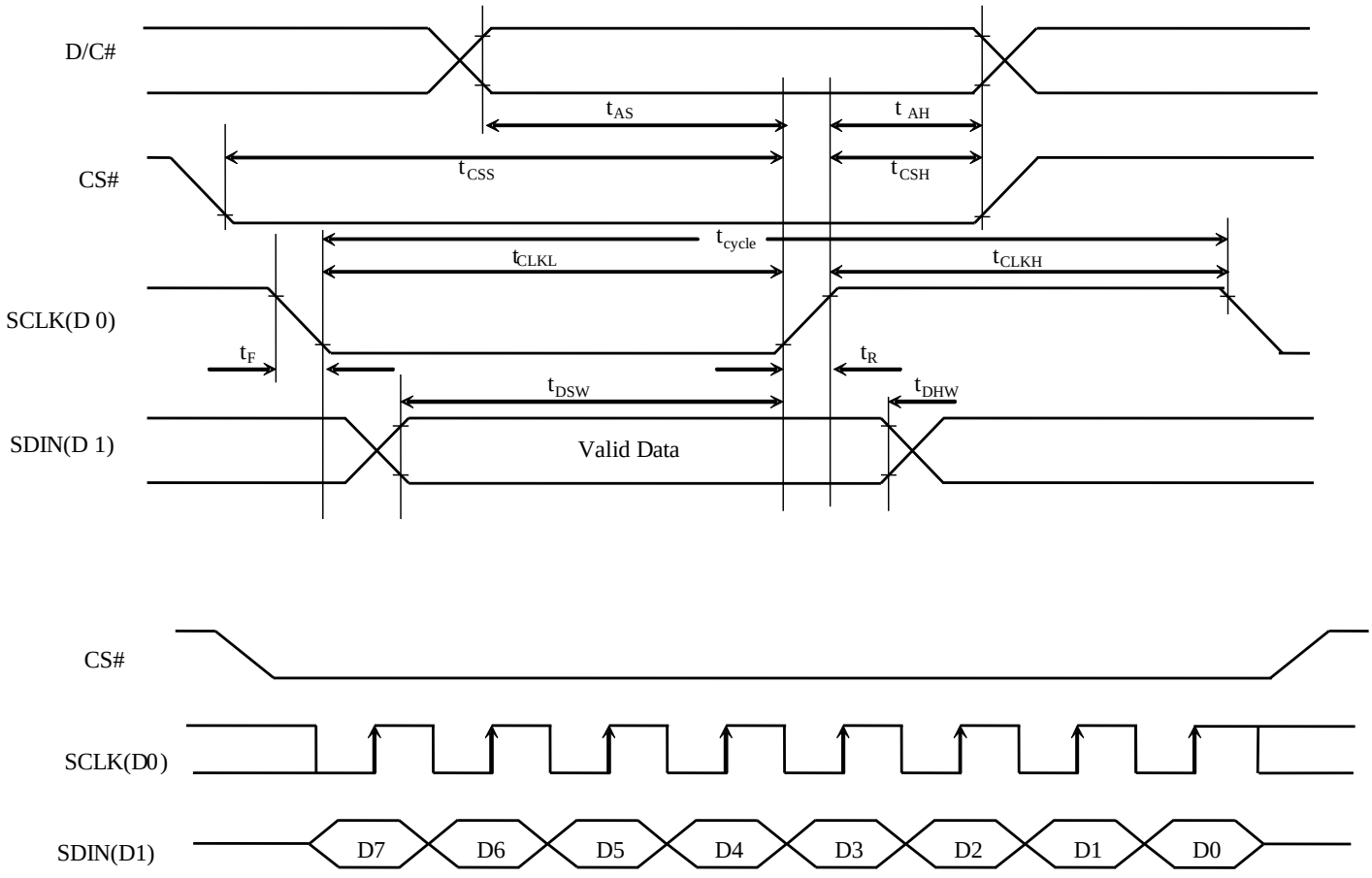
The Serial Peripheral Interface Timing Characteristics is shown in Table 12-2 and Figure 12-1:

Table 12-2 : Serial Peripheral Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.7V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time [20% ~ 80%]	-	-	15	ns
t_F	Fall Time [20% ~ 80%]	-	-	15	ns

Figure 12-1 : Serial peripheral interface characteristics



12.2.2 I2C Interface

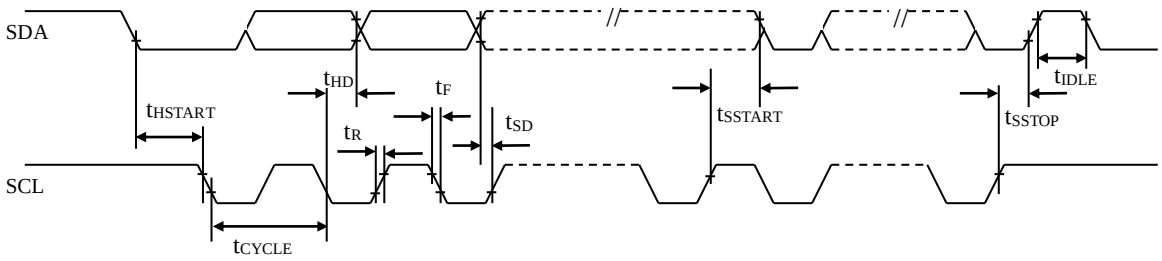
The I2C Interface Timing Characteristics is shown in Table 12-3 and Figure 12-2:

Table 12-3 :I2C Interface Timing Characteristics

(V_{DDIO} - V_{SS} = 2.4V to 3.7V, T_{OPR} = 25°C, C_L=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "TOUT1" pin)	0	-	-	ns
	Data Hold Time (for "D1" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Figure 12-2 : I2C interface Timing characteristics



13 APPLICATION CIRCUIT

Figure 13-1 : Booster Connection Diagram

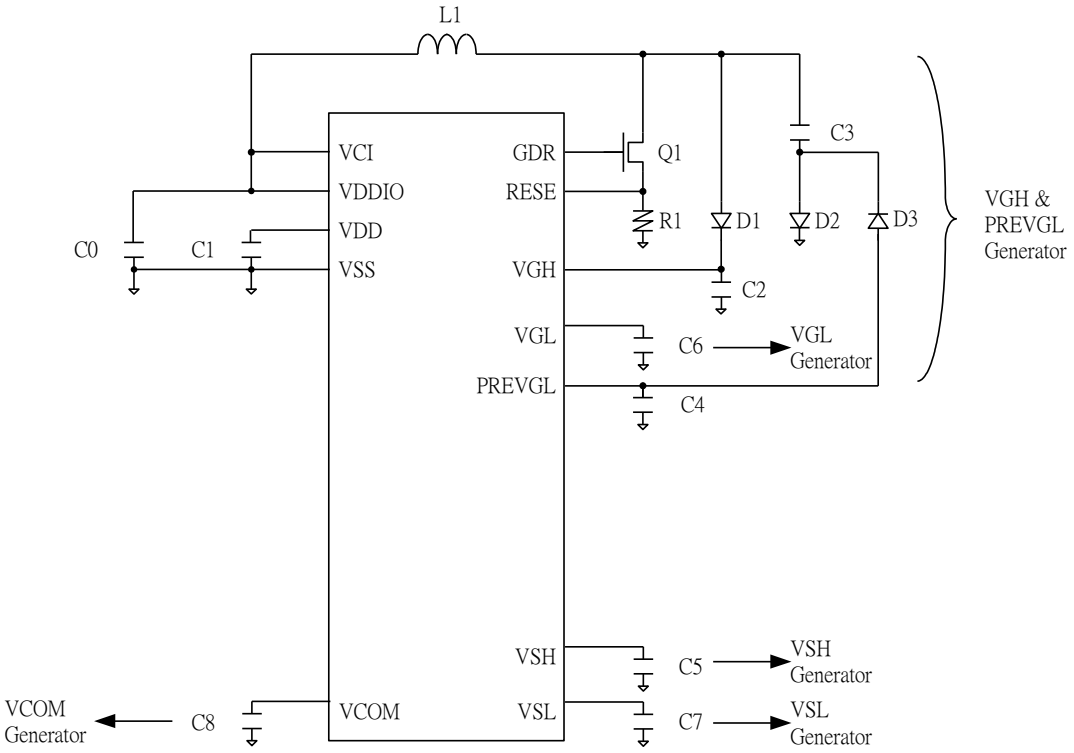


Table 13-1 : Reference Component Value

Part Name	Value	Max Volt. Rating [In V]	Pins Connected	MAX COG ITO resistance [in Ohm]
C0	1uF	6	VCI, VDDIO, VSS	5
C1	1uF	6	VDD, VSS	30
C2	1uF	50	VGH	5
C3	1uF	50	L1 and D2/D3	NA
C4	1uF	50	PREVGL	5
C5	1uF	25	VSH	5
C6	1uF	25	VGL	10
C7	1uF	25	VSL	5
C8	1uF	6	VCOM	5
L1	47uH			
Q1	NMOS [Vishay: Si1304BDL]		GDR, RESE	5
D1	Diode [OnSemi: MBR0530]		VGH	NA
D2	Diode [OnSemi: MBR0530]			NA
D3	Diode [OnSemi: MBR0530]		PREVGL, VSS	NA
R1	2.2 Ohm		RESE	5

14 PACKAGE INFORMATION

14.1 DIE TRAY DIMENSIONS

Figure 14-1 : IL3895 die tray information